WHAT IS CLAIMED IS:

1. A method of carrying out arbitration in a packet exchanger including an input buffer temporarily storing a packet having arrived at an input port, and a packet switch which switches a packet between a specific input port and a specific output port, said method comprising the steps of:

(a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order; and

(b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another.

2. The method as set forth in claim 1, wherein each of said basic processes includes the step of (c) selecting an output port through which a packet is output from an input port, among output ports not yet occupied by any input buffers, said step being to be carried out in input sequential arbitration in which said basic processes are carried out for said input buffers in a predetermined order.

3. The method as set forth in claim 1, wherein each of said basic processes includes the step of selecting an input buffer to be allowed to output a packet through an output port, among input buffers not yet allowed to do so, said step being to be carried out in output sequential arbitration in which said basic processes are carried out for said output ports in a predetermined order.

4. The method as set forth in claim 1, wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet,

said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

5. The method as set forth in claim 1, further comprising the step of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out.

6. The method as set forth in claim 5, wherein said second plurality of sequences is carried out in an order just opposite to an order in which said first plurality of sequences is carried out.

7. The method as set forth in claim 5, wherein said first plurality of sequences starts being carried out at a first time and said second plurality of sequences starts being carried out at a second time later than said first time by a predetermined period of time.

8. The method as set forth in claim 3, wherein each of said basic processes includes the steps of:

(a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers; and

(b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers.

9. The method as set forth in claim 8, wherein said step (a) is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet, and said step (b) is completed in a half of said unit period of time.

10. The method as set forth in claim 2, wherein said step (c) includes the steps of:

(c1) carrying out said basic processes for all of said input buffers with

respect to a packet having a higher priority; and

(c2) carrying out said basic processes for all of said input buffers with respect to a packet having a lower priority.

11. The method as set forth in claim 10, wherein each of said basic processes is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

12. The method as set forth in claim 10, wherein each of said basic processes is completed in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and wherein another sequence starts being carried out after said step (c1) have been completed.

13. The method as set forth in claim 1, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

14. An arbiter circuit constituting a packet exchanger together with an input buffer temporarily storing a packet having arrived at an input port, and a packet switch which switches a packet between a specific input port and a specific output port, said arbiter circuit having functions of:

(a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order; and

(b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another.

15. The arbiter circuit as set forth in claim 14, wherein an output port through which a packet is output from an input port is selected among output ports not yet occupied by any input buffers in each of said basic processes which

are carried out for said input buffers in a predetermined order.

16. The arbiter circuit as set forth in claim 14, wherein an input buffer to be allowed to output a packet through an output port is selected among input buffers not yet allowed to do so in each of said basic processes which are carried out for said output ports in a predetermined order.

17. The arbiter circuit as set forth in claim 14, wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet,

said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

18. The arbiter circuit as set forth in claim 14, wherein said arbiter circuit further includes a function of concurrently carrying out a second plurality of sequences after carrying out said first plurality of sequences.

19. The arbiter circuit as set forth in claim 18, wherein said arbiter circuit carries out said second plurality of sequences in an order just opposite to an order in which said arbiter circuit carries out said first plurality of sequences.

20. The arbiter circuit as set forth in claim 18, wherein said arbiter circuit starts carrying out said first plurality of sequences at a first time and said second plurality of sequences at a second time later than said first time by a predetermined period of time.

21. The arbiter circuit as set forth in claim 16, wherein said arbiter circuit selects an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers, and then selects an input

buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers, in each of said basic processes.

22. The arbiter circuit as set forth in claim 21, wherein said arbiter circuit selects said input buffer in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

23. The arbiter circuit as set forth in claim 15, wherein said arbiter circuit carries out said basic processes for all of said input buffers firstly with respect to a packet having a higher priority, and secondly with respect to a packet having a lower priority.

24. The arbiter circuit as set forth in claim 23, wherein said arbiter circuit carries out each of said basic processes in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

25. The arbiter circuit as set forth in claim 23, wherein said arbiter circuit carries out each of said basic processes in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and starts carrying out another sequence after said basic processes have been completed.

26. The arbiter circuit as set forth in claim 14, wherein said arbiter circuit includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes; and

(b) a signal line connecting said unit modules to one another in a ring.

27. The arbiter circuit as set forth in claim 14, wherein said arbiter circuit

includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes;

(b) a first signal line connecting said unit modules to one another in a ring, a signal being transmitted through said first signal line in a first direction; and

(c) a second signal line connecting said unit modules to one another in a ring, a signal being transmitted through said second signal line in a second direction opposite to said first direction.

28. The arbiter circuit as set forth in claim 14, wherein said arbiter circuit includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes;

(b) a first signal line connecting said unit modules to one another in a ring, a signal having a higher priority being transmitted through said first signal line; and

(c) a second signal line connecting said unit modules to one another in a ring, a signal having a lower priority being transmitted through said second signal line.

29. The arbiter circuit as set forth in claim 14, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

30. A recording medium readable by a computer, storing a program therein for causing a computer to carry out a method of carrying out arbitration in a packet exchanger including an input buffer temporarily storing a packet having arrived at an input port, and a packet switch which switches a packet between a

specific input port and a specific output port, said method comprising the steps of:

(a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order; and

(b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another.

31. The recording medium as set forth in claim 30, wherein each of said basic processes includes the step of (c) selecting an output port through which a packet is output from an input port, among output ports not yet occupied by any input buffers, said step being to be carried out in input sequential arbitration in which said basic processes are carried out for said input buffers in a predetermined order.

32. The recording medium as set forth in claim 30, wherein each of said basic processes includes the step of selecting an input buffer to be allowed to output a packet through an output port, among input buffers not yet allowed to do so, said step being to be carried out in output sequential arbitration in which said basic processes are carried out for said output ports in a predetermined order.

33. The recording medium as set forth in claim 30, wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet,

said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

34. The recording medium as set forth in claim 30, wherein said method

further includes the step of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out.

35. The recording medium as set forth in claim 34, wherein said second plurality of sequences is carried out in an order just opposite to an order in which said first plurality of sequences is carried out.

36. The recording medium as set forth in claim 34, wherein said first plurality of sequences starts being carried out at a first time and said second plurality of sequences starts being carried out at a second time later than said first time by a predetermined period of time.

37. The recording medium as set forth in claim 30, wherein each of said basic processes includes the steps of:

(a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers; and

(b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers.

38. The recording medium as set forth in claim 37, wherein said step (a) is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet, and said step (b) is completed in a half of said unit period of time.

39. The recording medium as set forth in claim 31, wherein said step (c) includes the steps of:

(c1) carrying out said basic processes for all of said input buffers with respect to a packet having a higher priority; and

(c2) carrying out said basic processes for all of said input buffers with

respect to a packet having a lower priority.

40. The recording medium as set forth in claim 39, wherein each of said basic processes is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

41. The recording medium as set forth in claim 39, wherein each of said basic processes is completed in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and wherein another sequence starts being carried out after said step (c1) have been completed.

42. The recording medium as set forth in claim 30, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

43. A recording medium readable by a computer, storing a program therein for causing a computer to act as an arbiter circuit constituting a packet exchanger together with an input buffer temporarily storing a packet having arrived at an input port, and a packet switch which switches a packet between a specific input port and a specific output port, said arbiter circuit having functions of:

(a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order; and

(b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another.

44. The recording medium as set forth in claim 43, wherein an output port through which a packet is output from an input port is selected among output ports not yet occupied by any input buffers in each of said basic processes which

are carried out for said input buffers in a predetermined order.

45. The recording medium as set forth in claim 43, wherein an input buffer to be allowed to output a packet through an output port is selected among input buffers not yet allowed to do so in each of said basic processes which are carried out for said output ports in a predetermined order.

46. The recording medium as set forth in claim 43, wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet,

said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

47. The recording medium as set forth in claim 43, wherein said arbiter circuit further includes a function concurrently carrying out a second plurality of sequences after carrying out said first plurality of sequences.

48. The recording medium as set forth in claim 47, wherein said arbiter circuit carries out said second plurality of sequences in an order just opposite to an order in which said arbiter circuit carries out said first plurality of sequences.

49. The recording medium as set forth in claim 47, wherein said arbiter circuit starts carrying out said first plurality of sequences at a first time and said second plurality of sequences at a second time later than said first time by a predetermined period of time.

50. The recording medium as set forth in claim 45, wherein said arbiter circuit selects an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers, and then selects an

input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers, in each of said basic processes.

51. The recording medium as set forth in claim 50, wherein said arbiter circuit selects said input buffer in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

52. The recording medium as set forth in claim 44, wherein said arbiter circuit carries out said basic processes for all of said input buffers firstly with respect to a packet having a higher priority, and secondly with respect to a packet having a lower priority.

53. The recording medium as set forth in claim 52, wherein said arbiter circuit carries out each of said basic processes in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

54. The recording medium as set forth in claim 52, wherein said arbiter circuit carries out each of said basic processes in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and starts carrying out another sequence after said basic processes have been completed.

55. The recording medium as set forth in claim 53, wherein said arbiter circuit includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes; and

(b) a signal line connecting said unit modules to one another in a ring.

56. The recording medium as set forth in claim 53, wherein said arbiter

circuit includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes;

(b) a first signal line connecting said unit modules to one another in a ring, a signal being transmitted through said first signal line in a first direction; and

(c) a second signal line connecting said unit modules to one another in a ring, a signal being transmitted through said second signal line in a second direction opposite to said first direction.

57. The recording medium as set forth in claim 53, wherein said arbiter circuit includes:

(a) a plurality of unit modules each associated with at least one of said input buffer and said output port, each of said unit modules carrying out said basic processes;

(b) a first signal line connecting said unit modules to one another in a ring, a signal having a higher priority being transmitted through said first signal line; and

(c) a second signal line connecting said unit modules to one another in a ring, a signal having a lower priority being transmitted through said second signal line.

58. The recording medium as set forth in claim 53, wherein the number of said sequences is equal to the number of ports in said packet exchanger.